

**DIGITAL-DISPLAY INTERFACES ARE THE FUTURE, BUT MOST MONITORS AND GRAPHICS ADAPTERS STILL USE ANALOG TECHNOLOGY. INTEGRATING BOTH ANALOG AND DIGITAL INTERFACES INTO YOUR DISPLAY GUARANTEES ITS COMPATIBILITY.**

# Bringing displays into the digital future

**T**HE MARKET DEMAND for flat-panel displays has steadily expanded over the last few years. Desktop monitors are benefiting from new technology, causing prices for flat-panel displays to drop. These products are increasingly attractive to consumer and corporate PC users.

Flat-panel displays, especially those with high resolution, need to maintain compatibility with the analog-RGB interface while adopting emerging digital standards. Achieving superior performance requires an understanding of high-speed mixed-signal design, which is crucial in solving technical problems specific to each interface. Analog Devices (www.analog.com) developed the AD9887 Dual Interface to bridge this technology gap.

The primary workhorse in display technology is the CRT, which requires RGB analog signals to display graphics data. A large legacy of PC-graphics adapters exists that uses RAMDACs to convert digital-graphics data to analog-RGB signals. The new flat-panel displays must be able to interface with this conventional technology to achieve greater market penetration and faster acceptance. However, emerging interface technologies based on high-speed serial-digital links offer solutions that allow flat-panel-display manufacturers to produce displays that are ultimately simpler to use.

In an effort to establish an industrywide standard for next-generation flat-panel displays, the DDWG (Digital-Display Working Group) developed the DVI (digital-visual-interface) specification. This specification outlines how designers should implement analog and digital interfaces. The analog timings reference the VESA (Video Electronics Standards Association) standard for computer-display monitors, and the digital interface uses the TMDS (transition-minimized-differential-signaling) format. Flat-panel-display manufacturers have discovered the market need to support the analog-RGB and digital interfaces in new designs. This dual-in-

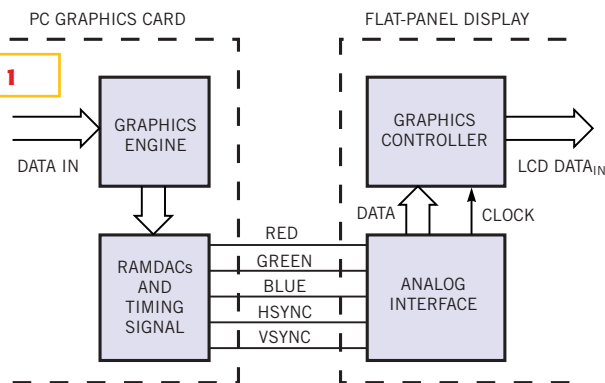
terface support would enable manufacturers to claim compliance with the DVI specification for their new flat-panel displays. Achieving effective system designs that can support both analog- and digital-interface formats is not as simple as it seems. Technical challenges exist in implementing an integrated design, which supports the complete DVI-I standard with both analog and digital interfaces in one monitor. You need experience in designing ADCs, low-jitter clock synthesizers, and high-speed serial-communications links if you want to achieve superior image quality.

## ANALOG OR DIGITAL?

To send graphics data from a PC to a flat-panel display, the data must be in either analog-RGB or digital formats. Although these formats of transmitting data to a flat-panel display differ conceptually, they perform similar operations in the system to receive and extract data and timing information.

In the analog-RGB format, the PC-graphics card sends data as a 256-level PAM (pulse-amplitude-

**Figure 1**



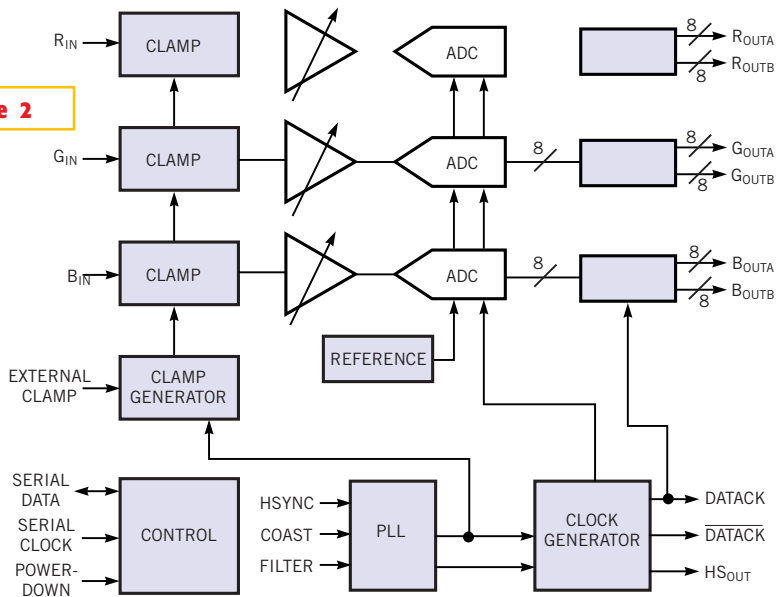
**An analog-RGB interface sends red, green, and blue image data along with HSYNC and VSYNC, synchronizing signals to a display.**

modulation) signal at the pixel-frequency rate. The graphics card uses DACs clocked at a predetermined pixel rate, based on the resolution, and converts the digital data into a sampled analog waveform. The flat-panel display receives this data and uses high-speed ADCs to convert it to digital format for further processing. This operation requires the recovery of the original pixel-clock frequency and phase so that the display samples the waveform at the correct rate and phase to reconstruct the data. The original phase of the graphics signal can get lost as it travels across a cable with unknown delay. Therefore, you need to recover the phase of the pixel clock so that you can correctly digitize the graphics signal.

With DVI, the PC-graphics subsystem encodes the original 8-bit graphics data to the serial DVI data stream, which consists of 10-bit, dc-balanced, transition-minimized words. This process indicates that the frequency of the data sent across the cable is 10 times the pixel-clock frequency. The DVI graphics card sends the pixel clock as a separate signal to the display. The display extracts the original data by recovering the clock's frequency and phase and then decodes the data to the original pixel value. The basic functions that either interface requires consist of decoding the received signal to the original digital format using timing signals generated through frequency and phase-recovery steps.

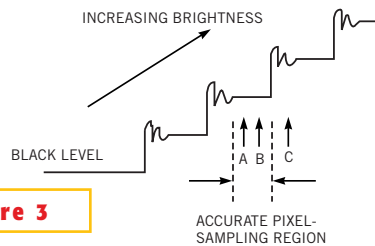
**IN SYNC WITH RGB**

Graphics adapters that send data from the PC to the display via analog-signaling methods use DACs to convert digital-graphics information to equivalent ana-



**Figure 2**

An analog flat-panel-display interface includes 8-bit ADCs, dc-restoring clamps, a pixel-clock synthesizer, and a data formatter.



**Figure 3**

Points A and B correctly sample the pixel value. Point C incorrectly samples the pixel value during the DAC's settling time.

log signals of 0 to 0.75V for the RGB channels. The adapter also sends the synchronizing signal's HSYNC, which identifies the beginning of a line on the dis-

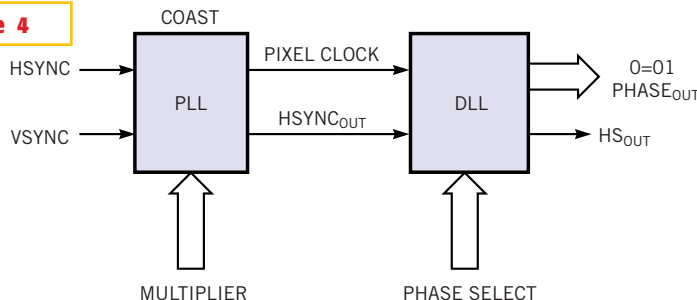
play, and VSYNC, which identifies the beginning of a new frame, to the monitor for proper operation (Figure 1).

The essential requirements of an analog flat-panel-display interface include three 8-bit ADCs with gain and offset adjustment for the RGB channels, a dc-restoring clamp circuit, a clock synthesizer for generating the reference pixel clock from the HSYNC signal, a pixel-clock-phase adjustment, and output-data formatting (Figure 2).

Using a pixel clock generated from HSYNC and a frequency-multiplying PLL, the 8-bit ADCs receive and digitize the RGB signals. The frequency response of the ADC front end is an important aspect of the signal chain. The input circuitry must be able to handle signal transitions with large dynamic range without lowpass-filtering the signal. In addition, the differential-nonlinearity performance of the ADC is important. Typically, you need an 8-bit ADC to exhibit a differential nonlinearity performance of a maximum of 1.5 LSB. If the differential-nonlinearity becomes larger than 1.5 LSB, then image quality begins to suffer, especially when it displays continuous shades of gray. You can control brightness and contrast by adjusting the offset and the gain of the ADC.

By ac-coupling the RGB signals to the

**Figure 4**

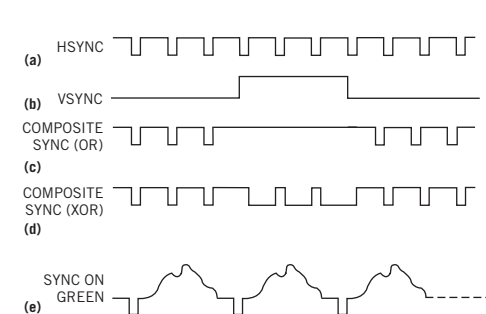


The clock generator for an analog interface uses a PLL to recover the pixel clock from the HSYNC signal and a DLL to set the sampling phase.

ADCs, you can remove the signals' dc level. Restoring dc to the *black* level of the signal allows correct conversion of the signal to proceed. You can accomplish this task by clamping the input-graphics signals to the black level, which is on the signal's "back porch" (the portion of the signal between HSYNC and the start of visible data). In RGB-graphics data, the black level is 0V. Other video formats, such as YUV, may require clamping two of the three channels to the midscale voltage of the converter. The AD9887 allows you to clamp the input signal to either ground or the midscale voltage to accommodate RGB- and YUV-graphics sources. The AD9887 also allows you to use an internally generated clamp signal with programmable placement and duration or an external clamp signal if you want to provide your own.

The accurate sampling and conversion of pixels requires a time-stable pixel clock. In other words, the pixel-clock synthesizer must have superior jitter performance. "Jitter" refers to the random time variations that clock-signal edges can experience due to device noise, power supply, or other disturbances. You have a finite amount of time to accurately sample the pixel (Figure 3). An advantage of sampling a pixel with more than one phase is that it gives flat-panel-display manufacturers a margin of adjustment in their designs. However, this sampling is possible only if the jitter of the pixel clock from which the phases are generated is low enough for more than one phase to sample a noisy pixel. The pixel-clock-generation subsystem has a frequency-multiplying PLL (phase-locked-loop) to recover the pixel clock from incoming HSYNC pulses (Figure 4). The DLL (delay-locked-loop)-based phase adjuster sets the sampling phase, which the graphics controller determines algorithmically.

The principle source of jitter in this system is the PLL frequency multiplier. The other sources are the VCO and the interaction of the HSYNC input with the PLL. The means of minimizing each of these sources of jitter differs. You minimize the VCO jitter through careful circuit-design techniques, resulting in VCOs that are less sensitive to device noise and power-supply variations. Sta-



**Figure 5** A flat-panel-display interface should handle the various sync formats that PC-graphics adapters use.

bility over the operating-temperature range ensures that the PLL dynamics do not change with temperature variations. However, minimizing jitter from the input HSYNC is a function of the PLL bandwidth. Because PLLs correct the phase error between the input signal and the VCO signal (the frequency of both signals being equal), the transfer function is both a ratio of output phase to input phase as a function of frequency and low-pass in nature.

The loop bandwidth is, therefore, the frequency at which phase variations at higher frequencies at the input are attenuated at the output. To make the PLL output signal less sensitive to input jitter, you need to make the loop bandwidth as narrow as possible. However, implications to overall jitter exist based on long-term locally generated VCO jitter. By narrowing the bandwidth, you limit the PLL's ability to correct some of the long-term jitter effects from the VCO. Narrowing the bandwidth to zero is the same as having the VCO running open-loop with no phase corrections possible, allowing it to drift. You want to maximize the bandwidth without sacrificing PLL stability so that the PLL corrects the long-term or accumulated errors. Therefore, a trade-off exists in setting the loop bandwidth between minimizing input-jitter effects versus cleaning up the long-term jitter effects from the VCO. Because the HSYNC signal is not a jitter-free signal and varies with each graphics adapter, a closed-form answer to setting the bandwidth is difficult to provide. To maximize performance over a range of graphics resolutions, or frequencies, the AD9887 allows some adjustment of loop bandwidth through the discrete adjustment of

the charge-pump current and the frequency range of the VCO. By adjusting these parameters, you can set the bandwidth of the PLL so that the typical jitter is less than 5.5% of the pixel-clock period over a 15- to 140-MHz operating range.

While digitizing the analog-graphics signal, the time point at which you take the sample is important because the DAC output exhibits some overshoot and ringing, which requires time to settle. The AD9887 produces 32 discrete phase options over an entire pixel period, corresponding to clock-phase edges separated by 11.25°. Note that phase options can cause significant conversion error from the actual pixel value. The phase-adjusting circuitry allows adjustment of the time position of the pixel clock so that accurate sampling of the pixel can occur, which also places a strict requirement on the input bandwidth of the ADCs. If the input bandwidth is too narrow, then the sampled analog-graphics signal is filtered so that accurate recovery of the original signal may be impossible.

PC-graphics adapters use different formats to send the HSYNC and VSYNC signals to the display. One format sends the HSYNC and VSYNC signals separately (figures 5a and b). In the composite HSYNC formats, the adapter embeds the VSYNC signal by ORing or XORing the HSYNC and VSYNC signals (figures 5c and d). The SOG (sync-on-green) format places the sync signal on the green channel (Figure 5e). Handling these different formats in a flat-panel-display or projector design is desirable. The composite HSYNC and SOG formats require circuitry that generates the full level HSYNC and VSYNC signals. For the SOG format, you need a sync slicer to extract the sync-tip information from the green channel. For both SOG and composite HSYNC formats, you need circuitry for separating the VSYNC from the composite signal.

When you use SOG or composite SYNCs, signal changes occur around the VSYNC period; the PLL should not respond to these changes in generating the pixel clock. The PLL's VCO must remain at the same frequency and not glitch or change frequency during those times. Therefore, the PLL in the frequency mul-

tiplier must be able to coast, or “fly-wheel,” through this period so that when the next legitimate HSYNC pulse arrives, the PLL picks up where it left off. If you improperly handle this problem, the image may display a “tearing” effect, usually at the upper left-hand corner, which is unacceptable. Designing an analog interface with good image quality at all graphics resolutions requires system components, such as ADCs and PLL-based clock-generation circuitry, with superior dynamic performance. To design an interface with discrete ADCs and PLLs, you need experience with high-speed mixed-signal design. However, such a design is usually costly in an industry that is cost-sensitive. Having the nuts and bolts of an analog-RGB interface that is integrated in one device is preferable.

#### DVI: THE NEW KID

Using serial-digital links to transmit formatted graphics data to flat-panel displays has become increasingly attractive to the producers of these products. The DVI specification endorses the TMDS interface and is the most popular interface. However, other available digital-interface formats are LVDS (low-voltage differential signal) and GVIF (gigabit video interface).

Figure 6 shows the system architecture for a DVI link. The graphics card sends pixel data across the link over Channel 2, or red; Channel 1, or green; and Channel 0, or blue. The card sends the clock on a separate channel and encodes the horizontal and vertical sync signals on the blue channel during blanking periods. You can also send additional control information on the red and green channels during blanking periods. The graphics system uses low-amplitude differential signaling, which offers improved common-mode noise rejection.

You should minimize the transitions of graphics data during transmission. The DVI encoding algorithm translates 8 bits of graphics data into a 10-bit word that is, in theory, transition-minimized. In addition, the transmission of long strings of ones can effectively charge up the cable to a higher dc voltage. Because the channel has limited bandwidth, it is difficult for a

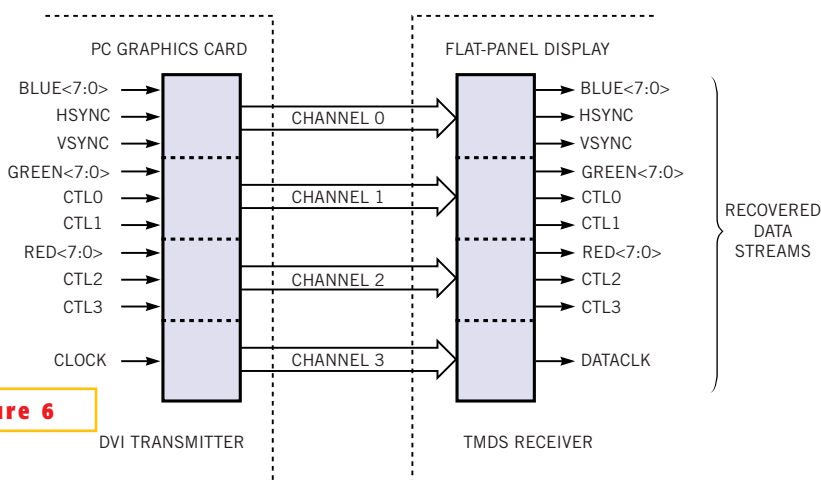


Figure 6

The DVI physical layer sends RGB pixel data and the clock over separate channels.

zero bit in a long chain of ones to quickly enough pull the voltage down to cross the comparator threshold and be detected as a zero. To minimize the intersymbol-interference problems associated with such a scenario, the DVI algorithm further encodes the data to achieve dc balancing of the cable. This balancing also allows you to use the system in fiber optics or other ac-coupled communication channels.

The algorithm encodes the data by counting the number of transitions in the data word. If this number is greater than four, then certain bits are inverted. For example, if the input word is 01010101, the encoded word is 00110011. To indicate that this inversion occurred, the algorithm adds a ninth bit and sets it to a one. In the previous example, the word becomes 100110011. The encoded word has a slight dc offset, but other encoded words in the library have worse offsets. The dc level of the transmitted words is monitored in the transmitter and attenuated by polarity reversal of the bits. Therefore, the dc balancing adds a 10th bit to the word, signifying whether the data is polarity-inverted. In actual operation, the

transmitter inverts every other word. For example, a sequence of three encoded words may be 0100110011, 1111001100, 0100110011.

As a result of the transmission of these words, the dc level of the cable remains at approximately 0V. The receiver uses the ninth and 10th data bits to restore the data to its original value.

The DVI sends the HSYNC and VSYNC information as control words on Channel 0 (blue) during the inactive data portion of the graphics transmission or blanking time. During this time, the transmitter sends one of four control words, depending on the state of the sync signals (Table 1).

The only time the interface does not minimize transitions is during the transmission of these control words. In fact, they are transition-maximized. The phase-recovery system uses these single-bit transitions to adjust or recover the proper phase between data and sampling clocks. The DVI interface then decodes the sync-signal information from these control words for further processing and outputs them to the flat-panel display.

The DVI receiver requires at least four functions to correctly receive encoded data: capturing analog data from the cable, sampling clock frequency and phase recovery, recovering frame-sync recovery, and channel deskewing.

In a DVI system, the

TABLE 1—HSYNC AND VSYNC CONTROL WORDS

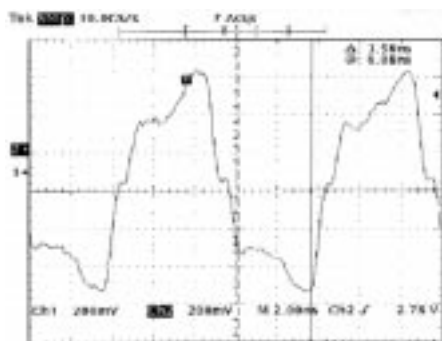
Data	Decodes to HSYNC <sub>OUT</sub>	And VSYNC <sub>OUT</sub>
10'b0010101010	0	1
10'b0010101011	0	0
10'b1101010100	1	0
10'b1101010101	1	1

transmitter sends data through a special-purpose 50Ω shielded twisted pair cable. Data rates can be as high as 1.65 Gbps, requiring signal-transition times of approximately 100 psec. Because the electrical length of the cable is approximately 8 nsec, you need to handle transmission-line effects. You also need to match the impedance of the receiver inputs to that of the cable so that reflections don't affect the accurate detection of data bits.

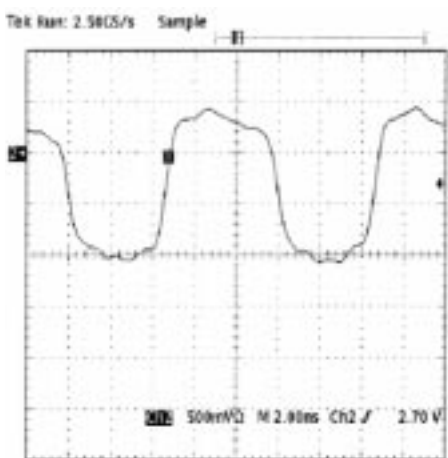
According to transmission-line theory, if you do not match impedances at the source or receiver ends of a transmission line to the characteristic line impedance, the signals will experience distortion due to reflections. A reflection is a portion of the voltage wave that is returned or reflected back to its source due to an impedance mismatch or discontinuity in the line.

When a digital pulse is sent down an improperly terminated transmission line, you can see a "step" in the pulse transition, from low to high voltage or vice versa. A DVI link's ability to detect 150-mV signals depends on how well-matched the input impedance of the receiver is to the cable. The oscilloscope waveform in **Figure 7** illustrates a serial bit-stream signal measured single-ended. The impedances are not well-matched in this example, as you can see by the steps in both pulse transitions. In contrast, **Figure 8** illustrates the same signal with the proper termination impedance. Notice the smooth transitions as the signal traverses the midpoint of its amplitude. Such smooth transitions are important for the input comparator to accurately determine the state of the signal during its measurement cycle. The AD9887 employs an on-chip termination system that tunes the value of the termination impedance based on an external reference resistance.

In any digital-communication system, you must recover sampling frequency and phase to properly sample the incoming symbols. The reference clock for DVI, which is one-tenth the bit rate, aids frequency recovery on the interface clock channel. However, a straight 10 times the frequency multiplication of the incoming clock frequency means internal clock rates can



**Figure 7** Poor termination can cause overshoot and undershoot as well as reflections in a DVI signal.



**Figure 8** Proper termination results in a smooth, clean DVI signal.

be as great as 1.65 GHz. This multiplication also implies that the sampling phase for each channel must be the same, which is inaccurate because delays on each channel are independent of one another. Therefore, an optimal phase for one channel may sample mainly noise on another channel, which means that you must do phase recovery on a per-channel basis. You can achieve a reasonable trade-off by doing frequency recovery on a global basis with an analog PLL and phase recovery on a per-channel basis with digital processing. Digitally recovering the phase requires that each symbol is oversampled, but oversampling poses a speed problem, because a straight 10-times multiplication can generate a 1.65-GHz clock. Oversampling by two times on each symbol requires a 3.3-GHz clock. One approach is to create an effective sampling clock

that multiple phases of a common clock generate. Assuming an oversampling rate of N, the effective clock frequency must be 10N. By generating equally spaced phases of this clock, you can divide the fundamental clock frequency by the number of phases created. If P represents the number of phases created, the fundamental clock frequency becomes

$$f_{\text{SAMPCLK}} = f_{\text{IN}} \left( \frac{10N}{P} \right)$$

The advantage of using higher oversampling is that you reduce static-sampling-phase offset. The drawback is that you must place more circuitry on the input to sample the data signal, which reduces the input bandwidth due to capacitive loading. The DVI specifies 100-psec rise times, which means that you need approximately 5 GHz of analog bandwidth to pass the pulses with minimal distortion.

When the system latches all of the oversampled bits, you can use various algorithms in parallel on the data to recover a near-optimal sample phase (2, 3), which is the desired data sample of the input bit.

When you use long cables, the transmission of digital data over three separate channels can result in considerable time skew between channels. The control words sent during inactive graphics provides a timing reference by which you can determine this skew. During normal operation, if a channel is skewed from the other two channels, digital logic initiates and executes a process that realigns the channels.

#### WHY NOT BOTH?

The current PC-installation base still uses an RGB-analog interface connected to a CRT display. Flat-panel displays should also have an analog interface to ease integration into this installed base. Although the graphics interface will eventually migrate to all-digital, the current availability of graphics adapters that are equipped with DVI digital transmitters is relatively nonexistent. Even notebook computers have a VGA connector for RGB-analog output. If a PC user pur-

chases a flat-panel display, then it must be able to plug into an analog interface. However, to ensure a future in the market, manufacturers should design displays that are DVI-compatible as well. Then users can employ a flat-panel display with any PC system.

The DVI specification acknowledges the need for a dual-interface strategy, which is why the specification uses the analog-RGB and digital interface. The DVI-I connector allows you to connect your monitor to either an analog-compatible or a DVI-compatible monitor.

Currently, flat-panel-monitor and projector designers provide dual-interface capability by using discrete parts, such as analog-interface ICs and discrete DVI digital receivers. This method is more costly because manufacturers have to use additional parts. They must also use more board space to accommodate the parts and the routing to connect them. In addition, designers have found that the image quality of flat-panel dis-

plays and projectors is highly dependent on board layout and design. Attempting to maintain the image quality across the two types of interfaces makes implementing this method more difficult. In addition, compact LCD projectors do not have the space to accommodate the larger pc-board area that discrete designs need.

The digital interface may be the future of linking PCs to flat-panel displays and projectors, but the analog interface is still the prevalent interface today. The level of integration in the AD9887 provides a clean and compact means of bridging the technological gap, making flat-panel displays and projectors usable with analog RGB today and ready for the digital interface in the future. □

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